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The Method of Solid State Impurity Diffusion and Doping In 4H-SiC

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ABSTRACT

Solid state thermal diffusion is not a common method of impurity doping in silicon carbide (SiC) device fabrication due to the extremely high temperatures required for such a process to occur. We have recently reported that solid state impurity doping by thermal diffusion in SiC is possible if there is a parallel mechanism, such as oxidation or silicidation that creates silicon or carbon vacancies, which then allows dopant impurities to diffuse into these vacancies. This paper describes the experimental procedures by which oxidation and silicidation can be used to generate vacancies and enhance impurity doping at temperatures below 1400 ºC.

Keywords: silicon carbide, impurity, doping, diffusion

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INTRODUCTION

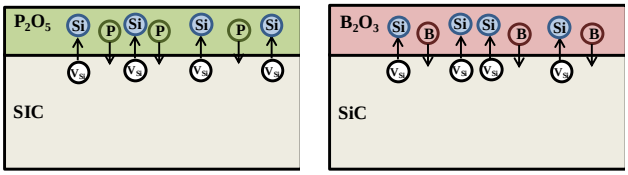
Silicon carbide (SiC) is an emerging wide band gap semiconductor which has been widely recognized as a suitable candidate to replace silicon as the preferred material for high power devices (Richmond, Hodge, & Palmour, 2004; Stephen, 2012; Willander, Friesel, Wahab, & Straumal, 2006). The wide band gap, high thermal conductivity, high critical electric field, and low-loss switching characteristics allow SiC devices to operate at higher temperatures, higher current density, higher blocking voltages, and higher energy efficiency than Si power devices. SiC technology has progressed to the point where commercial power devices are now available. However, SiC technology has yet to achieve maturity because of several issues in material and device processing (Agarwal & Haney, 2008; Matocha, 2008; Singh, 2006; Treu, Rupp, Blaschitz, & Hilsenbeck, 2006), such as high oxide-semiconductor interface defects, the need for low on-resistance. Formation of ohmic contacts in SiC device fabrication invariably requires ion-implantation and high temperature activation (Hallén et al., 2002), which are detrimental to surface quality. We have proposed an alternative method of doping that is possible at temperature below 1400 ºC.

The rate of impurity diffusion and the doping efficiency can be mediated or enhanced by vacancies. By intentionally creating vacancies, the process of impurity incorporation in a semiconductor can be controlled. Tin et al.(C. C. Tin, 2011) developed the vacancy assisted impurity doping (VAID) technique, which allows low temperature impurity incorporation in silicon carbide to occur. This technique requires an assisting mechanism that can create silicon or carbon vacancies, which then facilitate impurity incorporation in the lattice. Compelling data and thermodynamic arguments (Mendis et al., 2010; Tin et al., 2010) show that the general approach of vacancy creation to assist subsequent impurity doping is feasible. Oxidation and

silicidation are the two methods that have been studied for phosphorus and boron doping of 4H-SiC. Although boron doping is only marginally effective, phosphorus doping is remarkably effective using oxidation and silicidation due to the fact that the dopant source P_2O_5 is much less stable thermodynamically than the boron source B_2O_3 relative to SiO_2. The experimental procedures used for both techniques are described in detail in this paper in order to provide a coherent description to help in the understanding and implementation of the technique.

BASIC CONCEPTS

The general aim of oxidation or silicidation is to generate vacancies as shown in Figure 1. Figure 1a shows the use of P_2O_5 to produce n-type doping using phosphorus dopants. Figure 1b shows the use of B_2O_3 to produce p-type doping using boron dopants. The oxidation approach uses an oxide of an impurity such as B_2O_3 or P_2O_5 which is deposited on top of the 4H-SiC surface and heated to a sufficiently high temperature. This causes the silicon atoms in the silicon carbide to diffuse into the oxide layer to form silicon dioxide, leaving behind silicon vacancies. Because this reaction is exothermic, it facilitates the creation of vacancies, which in turn helps the impurity atoms in the oxide layer to diffuse into the near-surface region of the SiC and occupy the vacant silicon sites. In the figure, we have shown B atoms occupying silicon vacancies because B_{Si} is the preferred shallow-level defect for boron doping of SiC[9].



a b

Fig.1 Schematic diagram for (a) phosphorus (b) boron doping

Silicidation is an alternative method to create silicon vacancies and this method is much more efficient that oxidation. The silicidation assisted impurity doping technique uses a metal, such as nickel, as a catalyst for creating Si vacancies. Nickel is deposited as a thin on top of the impurity oxide layer. Figure 2 shows the probable mechanisms in the silicidation assisted impurity doping process.

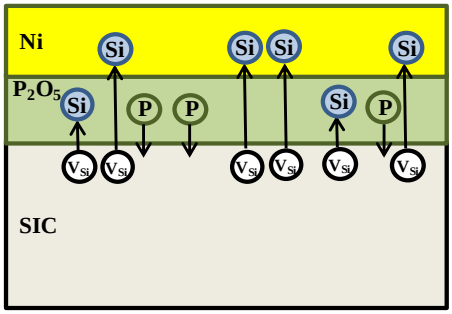


Fig.2 Schematic diagram for silicidation assisted impurity doping process for phosphorus

EXPERIMENTAL PROCEDURES

In this work, experiments were carried using 4H-SiC wafers diced into 5mm x 5mm samples. Both n- and p-type 4H-SiC were used for the fabrication and characterization of Schottky and ohmic contacts. The epitaxial layers of both the n-type and p-type samples had a background doping concentration of 10^{15}-10^{16} cm^{-3}. Semi-insulating 4H-SiC was mainly used for making samples for physical analysis, such as EDX, RBS and SIMS. There was no particular reason for using semi-insulating substrates other than it being available at the time.

SAMPLE CLEANING

Samples were first cleaned using both organic and RCA cleaning processes. Meticulous cleaning is essential to remove any kind of particulate matter on the surface of the sample, including traces of organic, ionic or metallic contaminants. Steps used in the cleaning process are listed below.

ORGANIC CLEAN

- Immerse in acetone for 5 min.
- Immerse in trichloroethylene (TCE) for 5 min.
- Immerse in acetone for 5 min.
- Immerse in methanol for 5 min.
- Rinse in de-ionized (DI) water.
- Immerse in buffer oxide etch (BOE) for 4 min.
- Rinse in DI water for 2 min and dry with N2 gas.

RCA CLEAN

- Immerse in a 1:1 solution of H_2O_2:H_2SO_4 for 15 min.
- Rinse with DI water for 2 min.
- Immerse in BOE for 1 min.
- Rinse with DI water for 2 min.
- Immerse in boiling 6:1:1 solution of DI water: H_2O_2: NH_4OH for 15 min.
- Rinse with DI water for 2 min.
- Immerse in BOE for 1 minute.
- Rinse with DI water for 2 min.
- Immerse in boiling 6:1:1 solution of DI water: H_2O_2: HCl for 15 min.
- Rinse with DI water for 2 min.
- Immerse in BOE for 1 minute.
- Rinse with DI water for 2 min.
- Dry with N2 gas.

PHOTOLITHOGRAPHY

Photolithography is a necessary process to transfer a particular pattern from a photomask onto a sample. This process requires a mask aligner. We used the Karl Suss MJB3 UV400 mask aligner. This manually-controlled mask aligner is equipped with an optical microscope having magnification by factors of 5, 10, and 20, as well as a Hg lamp that provides a UV light source with an output power of 160W. The resolution of the mask aligner is 2-3 μm.

The mask aligner is designed to accommodate a wafer with a maximum diameter of 4 in. Since each sample used in this work was only 5 mm x 5 mm in size, they were attached to the center of a 3-in silicon wafer using a water-soluble wax before photolithographic processing took place. The wafer, with the sample, was coated with photoresist (AZ 5214-EIR) using a spin-coater with a rotational speed of 4000 rpm for 30 s. The thickness of the photoresist layer on the sample was approximately 1.5 µm. The wafer was subsequently soft-baked for 1 min in an oven that was constantly maintained at 110 ºC. After soft-baking, the wafer was mounted on the mask aligner and the sample was aligned with the desired pattern on the mask. The sample was then exposed to ultraviolet (UV) light for 30 s. The final step in the photolithographic process was development, in which a mixture of DI water and chemical developer (AZ 400K) was used. While still mounted on the 3-in wafer, the samples were immersed in the developing solution for approximately 10-15 s, then rinsed in DI water for 1 min, and blow dried using N_2. During development, the area which was exposed to UV light dissolved, leaving behind the pattern of the mask on the sample.

METAL SPUTTER DEPOSITION

Metals were sputter-deposited using magnetron sputtering. The process took place in a high vacuum chamber capable of achieving approximately $3x10^{-7}$ Torr. The 5 mm x 5 mm samples, which were still attached to the 3-in Si wafer, were mounted on a circular holder which can be mechanically rotated to position directly above a specific sputter gun. During the sputtering process, Ar gas flow of about 100 sccm was used with the chamber pressure maintained at about 18 mTorr. The metal used was an alloy of 93% Ni/ 7% vanadium ($Ni_{93}V_7$), which was predominantly used as the ohmic contact metal, in this work. Before deposition, the target surface was cleaned by pre-sputtering for 2 min after which the sample was rotated into position for deposition. A total sputtering time of 8 min is used for ohmic contacts with a thickness of approximately 1500 Å.

THERMAL EVAPORATION

Thermal evaporation was usually carried out at a pressure of approximately 5×10^{-6} Torr. Ni can react with the tungsten boats causing the latter to break. Our approach was to use alumina-coated tungsten boats.

DIFFUSION ANNEALING

Dopant diffusion was carried out in an alumina furnace that was capable of achieving 1600 ºC. The samples were first cleaned using the standard organic and RCA cleaning processes. A dopant solution was spin-coated on the surface of the SiC sample at a speed of about 1500 rpm for phosphorus spin-on solution and 4000 rpm for the boron solution. Commercial spin-on dopants with no silica content, such as Filmtronics P450, were found to be more reliable and were usually used. Supersaturated boric oxide in methanol solution was also tried successfully. Figure 3 shows the process for phosphorus diffusion. After spinning the dopant solution onto the surface, the SiC sample was heated to 650°C in O_2 for 30 min, which led to the formation of a glassy P_2O_5 layer on the surface. The sample was then annealed in O_2 for 1 hr in the alumina furnace at a temperature ranging between 1200°C and 1400°C. The sample was allowed to cool to room temperature in the furnace. The sample was then removed from the furnace and immersed in buffered oxide etch (BOE) for 5 min to remove the phosphosilicate layer from the surface.

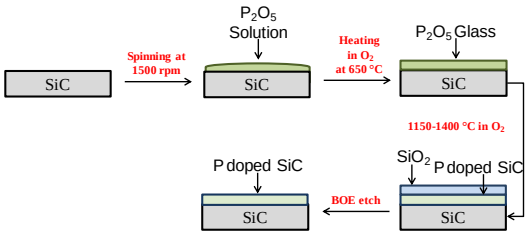


Fig. 3 Process for phosphorus diffusion

SILICIDATION ASSISTED IMPURITY DOPING

Figure 4 shows a variation of the above process where nickel was used as a catalyst for the dopant diffusion process. The phosphorus solution was spin-coated on the sample and heated in O_2 at 650°C to produce a P_2O_5 glassy layer. Then, pure nickel was thermally evaporated onto the sample using the thermal evaporation system. Subsequently, the sample was annealed in an Ar ambient at 900°C for 1 hr. After the sample was cooled to room temperature, it was immersed in BOE to remove the top nickel silicide/phosphosilicate layer. After removing the residual nickel silicide/phosphosilicate glass layer, the sample can be further annealed at higher temperature for greater activation.

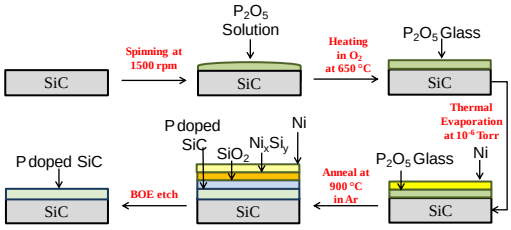


Fig.4 Process for silicidation assisted phosphorus diffusion.

BORON DIFFUSION

The boron oxide solution was spin-coated on the SiC at 4000 rpm. The speed can be varied depending on the viscosity of the dopant source. For our home-made boric oxide solution, boron oxide particles were observed to be uniformly deposited on the sample. The sample was then heated in O_2 at 650°C for 30 min in the alumina furnace to form a glassy B_2O_3 layer. The sample was subsequently annealed in O_2 for 1 hr in the alumina furnace at a temperature ranging between 1200°C and 1400°C. After the sample was cooled to room temperature, it was immersed in BOE to remove the top layer of borosilicate layer. The sample can be further annealed at higher temperature or

longer period for greater activation or greater diffusion depth. The boron diffusion process is shown in Figure 5.

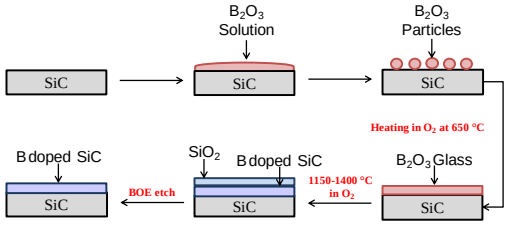


Fig. 5 Process for boron diffusion.

VACUUM ANNEALING

A rapid thermal annealing system (RTA) was used for both ohmic contact anneals and dopant activation anneals. The system used two thin carbon strips as the heating element. For ohmic contact annealing, the sample was clamped down on the carbon strip. No surface protection was necessary because contact annealing was usually done at about 1000 – 1200 ºC. $Ni_{93}V_7$ was the preferred metal for ohmic contacts for the phosphorus-doped SiC in this work. The ohmic contacts were usually annealed at temperatures of about 1100 ºC for 5 min in a vacuum of 2 x 10^{-7} Torr, with the samples clamped directly onto the carbon strip.

For dopant activation annealing, the sample was turned over with its face down and placed inside a SiC pill-box, which was then placed on the carbon strip. By using the SiC pill-box and by placing the face of the sample against the bottom of the SiC ensured that a silicon-rich atmosphere, or silicon overpressure, was formed to protect the surface from deterioration. This was necessary because activation annealing was carried out at a higher temperature of about 1400 – 1500 ºC although the maximum temperature achievable was about 1700 ºC. Dopant activation annealing was usually done in an argon atmosphere. Before annealing, the system was first evacuated to about 2 x 10^{-7} Torr, before introducing a steady Ar flow into the chamber. Activation annealing was usually carried out for 30 min.

REACTIVE ION ETCHING

Our reactive ion etching (RIE) process used NF_3 etchant gas in plasma produced by an RF voltage. Before the RIE procedure, nickel etch mask was photolithographically patterned for selective etching of the SiC. For 4H-SiC, an etch rate of 90 nm/min was attained using the NF_3 plasma at a chamber pressure of approximately 35 mTorr.

BASIC DEVICE FABRICATION PROCESS

The above-mentioned processes were employed to fabricate our test structures for electrical characterizations. Figure 6 shows the typical process to produce ohmic contacts on our diffusion-doped 4H-SiC samples.

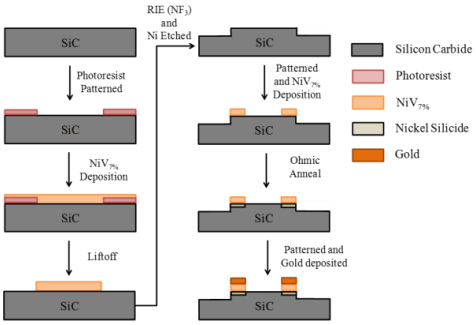


Fig.6 Process for ohmic contact fabrication

CONCLUSION

We have proposed a new method of solid state dopant diffusion using an assisting mechanism, such as oxidation or silicidation, to produce silicon or carbon vacancies. Our studies have shown that this technique is feasible and has valid thermodynamic justification. The outlines of the various experimental processes to produce our solid state impurity doping method were described to provide a coherent description and to help in the implementation of the technique.

REFERENCES

Agarwal, A., & Haney, S. (2008). Some critical materials and processing issues in SiC power devices. *Journal of Electronic Materials, 37*(5), 646-654.

C. C. Tin, A. V. A., I. G. Atabayev, B. G. Atabaev, T. M. Saliev, E. N. Bakhranov, M. Li, S. P. Mendis and C. A. Ahyi, , . (2011). U.S. Patent No.: 7, 268.

Hallén, A., Janson, M., Kuznetsov, A. Y., Åberg, D., Linnarsson, M. K., Svensson, B., . . . Bergman, J. (2002). Ion implantation of silicon carbide. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 186*(1), 186-194.

Matocha, K. (2008). Challenges in SiC power MOSFET design. *Solid-State Electronics, 52*(10), 1631-1635.

Mendis, S. P., Tin, C.-C., Saddow, S., Sanchez, E., Zhao, F., & Dudley, M. (2010). *Phosphorus Oxide Assisted n-type Dopant Diffusion in 4H-Silicon Carbide.* Paper presented at the Materials Research Society Symposium Proceedings.

Richmond, J., Hodge, S., & Palmour, J. (2004). Silicon carbide power applications and device roadmap. *Power Electronics Europe, 7*, 17-21.

Singh, R. (2006). Reliability and performance limitations in SiC power devices. *Microelectronics Reliability, 46*(5), 713-730.

Stephen, B. (2012). Silicon Carbide Technology Overview. *Journal of Electrical Engineering & Electronic Technology*.

Tin, C.-C., Mendis, S., Chew, K., Atabaev, I., Saliev, T., Bakhranov, E., . . . Adedeji, V. (2010). Oxide film assisted dopant diffusion in silicon carbide. *Thin Solid Films, 518*(24), e118-e120.

Treu, M., Rupp, R., Blaschitz, P., & Hilsenbeck, J. (2006). Commercial SiC device processing: Status and requirements with respect to SiC based power devices. *Superlattices and Microstructures, 40*(4), 380-387.

Willander, M., Friesel, M., Wahab, Q.-u., & Straumal, B. (2006). Silicon carbide and diamond for high temperature device applications. *Journal of Materials Science: Materials in Electronics, 17*(1), 1-25.

