Fundamental Journals
International Journal of Fundamental Physical Sciences (IJFPS) ISSN:2231-8186
IJFPS, Vol 4, No 2, pp 37- 42, June , 2014 Y.K. Sharma
DOI:10.14331/ijfps.2014.330064
http://dx.doi.org/10.14331/ijfps.2014.330064

Improved Stability of 4H Sic-MOS Devices after Phosphorous Passivation with Etching Process

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(*Received March 2014; Published June 2014*)

ABSTRACT

Phosphorous passivation of the interface (4H-SiC/SiO_2) improves interface trap density (D_{it}) from 10^{13} $eV^{-1}cm^{-2}$ to $2\times10^{12}eV^{-1}cm^{-2}$ at 0.2eV below the conduction band edge of 4H-SiC. Due to the formation of phosphosilicate glass (PSG) layer during P passivation, metal-oxide-semiconductor capacitors (MOS-Cs) are highly unstable. Under bias-temperature stress (BTS) there is very large shift in the flatband voltage, V_{FB}, (independent of the bias polarity) of MOS-Cs. In this paper we proposed a new method to improve the stability of these devices. The PSG layer formed after passivation is etched-off in buffered oxide etch (BOE) and then capped with deposited oxide. Devices fabricated with this process showed D_{it} of $4x10^{12}eV^{-1}cm^{-2}$, and are stable after BTS test performed at 150°C, +1.5MV/cm. This value of D_{it} is as good as the-state-of-the-art NO/N_2O passivated MOS-C. Also, XPS indicated the presence of P at the interface after etching which explains "NO/N_2O –like" D_{it} for etched PSG MOS-Cs.

Keywords: Silicon carbide, interface trap density, XPS, phosphosilicate glass

DOI:10.14331/ijfps.2014.330064

INTRODUCTION

SiC is best suited for high power devices due largely to its large band gap, high breakdown field and high thermal conductivity. SiC has three times the thermal conductivity of Si, and this is very important for power devices. Inefficient heat dissipation makes device behavior unpredictable, for example at higher temperatures a device can have higher leakage current, higher on-state resistance, and switch state from normally-off to normally-on. But higher thermal conductivity makes SiC a suitable material for high-power devices which can operate at temperatures >200°C.

In addition, high saturated electron velocity means that SiC is a good choice for microwave and radio frequency applications. SiC Schottky diodes have been on the market since 2001, and are proving to be reliable replacements for better than silicon junction diodes. Recently, CREE Inc. has also marketed 1700V SiC power MOSFETs (CREE, 2014). SiC can form a native thermal oxide and hence is well-suited for MOS technology. Unlike Si, SiC has complicated oxidation and etching chemistry (Xu et al., 2014). It has been suggested that formation of different carbon-related species during oxidation makes the channel region of 4H-SiC

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MOSFETs electrically resistive (Sharma et al., 2012). As-oxidized SiC has a very high interface trap density (D_{it}) in the energy of 0.1eV to 0.6eV beneath the conduction band (CB) of 4H-SiC. D_{it} can be reduced from 10^{13} $eV^{-1}cm^{-2}$ to $1x10^{12}eV^{-1}cm^{-2}$ at 0.2eV using standard NO (N_2O)/and nitrogen plasma passivation (Chung et al., 2001). Also it has been reported that a low interface trap density is possible after high-temperature (>1200^oC) oxidation (Kurimoto, Shibata, Kimura, Aoki, & Sugino, 2006).

Recent reports on phosphorus (P) passivation are very promising with D_{it} of 2-4x$10^{11}eV^{-1}cm^{-2}$ (Liu et al., 2013; Okamoto, Yano, Hatayama, & Fuyuki, 2010; Sharma et al., 2012; Zhang, 2013). Low D_{it} translates into high field-effect mobility of ~80cm^2/V.s. As shown in references (Sharma et al., 2013), P passivation leads to device instability due to the formation of PSG layer. In this paper we proposed a way to improve the stability of these devices while keeping the interface trap passivation effect of P.

MATERIALS AND METHODS (SAMPLE CLEANING)

Sample cleaning can be divided in to two parts-organic cleaning and Radio Corporation of America (RCA) cleaning.

ORGANIC CLEANING

Organic cleaning is done to remove oils and organic residues that appear on glass surfaces(Kern, 1991, 1993; Vossen & Kern, 1991). For SiC, the organic cleaning procedure uses acetone, trichloroethylene, acetone, and methanol. Each of the organic cleaning steps takes five minutes in an ultrasonic cleaner. Particles ranging in sizes from several micrometers to a tenth of a micron can be removed using ultrasonic waves(Kern, 1990). First acetone and trichloroethylene is used for complete organic degreasing. Second, acetone serves as the solvent to dissolve trichloroethylene, and methanol is the solvent for acetone. Finally, methanol is used to further clean organic solvents. The sample is then rinsed in deionized (DI) water and blown dry using nitrogen gas.

RADIO CORPORATION OF AMERICA (RCA) CLEANING

This cleaning is done to remove organic, ionic and metallic impurities from the sample (Kern, 1993; Vossen & Kern, 1991). First, the sample is immersed in buffered oxide etch (BOE) for five minutes to remove a thin layer of native oxide, and then it is rinsed in DI water. Next the sample is immersed in a piranha etch solution (H_2SO_4+H_2O_2) with a volume ratio of 1:1. The piranha etch is used to remove heavy organic materials such as photoresist and other visible contaminations of organic nature. The sample is rinsed well in DI water and immersed in BOE for one minute. The sample is rinsed again in DI water and immersed for 15min in a heated (~100^oC) solution of DI water, ammonium hydroxide and hydrogen peroxide (3:1:1). This solution dissolves many metallic contaminations: copper, for example, forms $Cu(NH_3)_4^{+2}$ amino-complex. The next step is again the cleaning sequence of DI water and BOE. To dissolve alkali ions and metal hydroxides, a strong acidic solution of DI water, hydrochloric acid, and hydrogen peroxide (3:1:1) is used for 15min at ~100^oC. Next the sample is rinsed in DI water and immersed in BOE for one minute. Finally, it is well rinsed in DI water and blow-dried using nitrogen gas.

OXIDATION

The performance of an MOS device critically depends upon the quality of the oxide layer. Of many oxidation processes, thermal oxidation is the process most commonly used to form the interface (SiC/SiO_2). Thermal oxidation is carried out in an oxygen (O_2) ambient (500sccm) at 1150^oC. A high purity quartz (GE 224) furnace tube was used for thermal oxidation, (Fig 1). The tube has gas inlets for O_2, N_2 and Ar. The furnace tube is 48in long, 4in in diameter with a maximum operating temperature of 1200^oC.

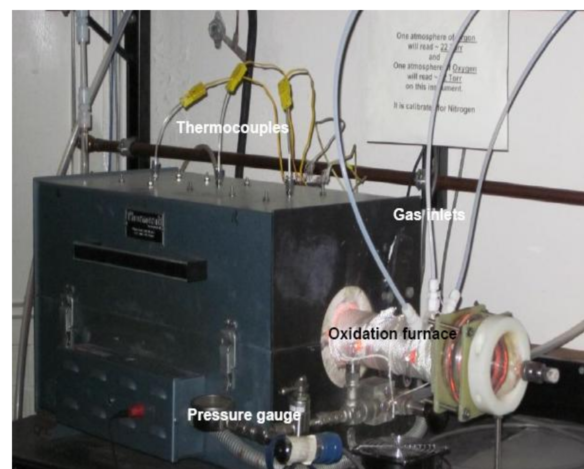

Fig.1 Thermal oxidation station

PHOTOLITHOGRAPHY

Photolithography is the most critical step during the device processing since this step defines the device dimensions and the resolution that can be achieved. Patterns are transferred from a photo-mask to a light sensitive chemical, photoresist, on the SiC sample. The 5mm×5mm (or 10mm × 10mm) sample is first attached to a three inch silicon wafer, using photoresist for a mechanical support. Shipley AZ5214E photoresist is spun on the sample for 30 seconds at 4,000 revolutions/minute to form a uniform layer of photoresist (1.5μm). The photoresist is prebaked at 110^oC for one minute, to make it UV light-sensitive. The sample is aligned under mask, and then it is exposed to a 160W ultra violet (UV) source for 30 seconds. The sample is developed in a 1:4 diluted AZ 400K developer for about 30 seconds.

SPUTTERING

Sputter deposition is performed at a low pressure (~100mT of Argon gas) in a vacuum chamber. Before deposition, the vacuum chamber is evacuated to a base pressure of $4x10^{-7}$Torr. Argon is introduced into the chamber at a flow rate of 100sccm, and the pressure in the chamber is stabilized to 20mTorr for five minutes. A pre-sputtering process is used to remove trapped impurities at the surface of the targets.

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Depending on the target metal, this process requires thirty seconds to five minutes. After pre-sputtering, the sample is positioned at about 4in above sputter target. Approximately 150nm of molybdenum is sputtered to from the contacts on MOS-C. 120 nm nickel-vanadium (Ni/V, 93/7 wt %) is sputtered to form ohmic contacts on the back of MOS-C after removing the oxide.

LIFT-OFF

Lift-off is the procedure that is used to pattern metal films on the sample. First, the pattern is defined on the sample by applying and exposing photo-resist. Metal is then sputtered all over the patterned sample. The sample is then exposed to acetone which is a solvent for the photoresist. The semiconductor surface where no metal is required is protected by the photoresist.

Acetone, in the process of dissolving the photoresist, also removes the metal deposited on top of it. Afterwards, the sample is washed with methanol to make sure that there is no remnant of acetone. Finally, it is rinsed in DI water and blow-dried using nitrogen gas. In addition, we used a low pressure chemical vapor deposition (LPCVD) system operating with tetraethylorthosilicate (TEOS) for SiO_2 deposition at 650°C (well below the temperature for thermal oxide growth on SiC). The etched MOS-C fabrication involved following steps:

i. Thermal oxidation of 4H-SiC.
ii. Phosphorus passivation at 1000°C to form a layer of PSG.
iii. Etching of PSG layer in BOE for 2- 3min.
iv. Deposition of an oxide layer using TEOS in a LPCVD system.
v. Densification of the deposited oxide layer (950°C, 2hr, 0.5L/min pure N_2)
vi. Sputtered deposition of Mo to form gate metal contacts.
vii. Backside ohmic contacts using $Ni_{93\%}V_{7\%}$.

RESULTS AND DISCUSSION

(i) SIMULTANEOUS HIGH-LOW C-V TEST

The simultaneous high-low frequency capacitance-voltage (C-V) method is employed to characterize MOS-Cs, especially the interface characteristics. Figure 2 shows the schematic of an N-/N+ MOS capacitor. A grounded black metal box is used for better insulation from stray magnetic/electric fields and from light. Electrical measurements are made with a Keithley 595 analyzer and a Keithley 590 CV meter.

The Keithley 590 CV meter measures the quasi-static capacitance and Keithley 595 analyzer measures the high-frequency capacitance. Both measurements are made concurrently. The bias voltage for the experiments is provided by a Keithley 230 programmable voltage source. These components are controlled using the Interface Characterization Software (ICS) package.

This package is designed to run the measurements, record the raw data, extract parameters and plot the results. During the measurement, the device is swept from accumulation to depletion using a slowly changing DC bias to obtain a quasi-static capacitance curve.

A high frequency signal, 100KHz for room temperature (1MHz for high temperatures C-V measurement), is applied simultaneously between the gate and back contact. The high frequency curve does not reflect the effects of interface traps and other possible defects, as they fill and empty at frequencies that are much lower compared to the 100kHz or 1MHz high frequency signal(Cooper Jr, 1997; Gupta, 2012).

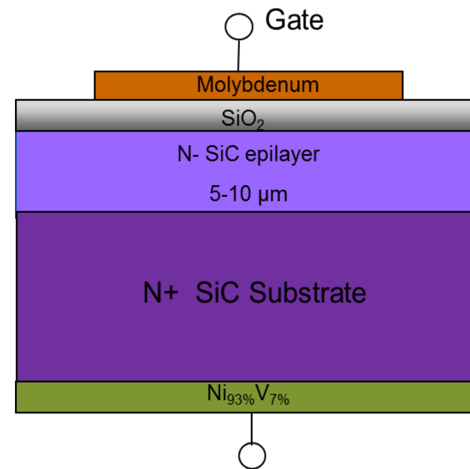

Fig.2 Schematic of an N-/N+ Metal Oxide Semiconductor (MOS) capacitor. In the case of PSG MOS-C the gate oxide is consists of PSG, while for the etched PSG MOS-C a deposited oxide is used after etching the PSG layer in BOE.

This high frequency C-V curve can therefore be assumed to be the theoretical ideal curve in calculations. For a given bias voltage (i.e., given position in the band gap and given interface trap energy), the separation between the quasi-static and high-frequency C-V curves determines the number of interface traps.

A typical high-low C-V curve for an etched N-type PSG MOS-C is shown in figure 3(a). The corresponding interface trap density is shown in figure 3(b) where the solid line represents the high-frequency capacitance (CH), and the dotted line represents the quasi-static capacitance (CQ).

The energy level of a trap in the band gap is determined by the position of the Fermi level at the silicon carbide surface for a given gate bias voltage.

Due to wide band gap of silicon carbide (3.2eV), only the interface traps with energies between E_c -0.6eV can respond to quasi-static signal at room temperature. From figure 3(b), it is clear that etching increases the interface trap density. Although, there is an increase in the trap density of etched PSG MOS-C, the D_{it} profile is similar to that of an unetched NO MOS-C (Fig 4).

D_{it} for the etched NO MOS-C is significantly higher and similar to the profile of as-oxidized (at 1150°C) MOS-C (Fig 3(b) and 4).

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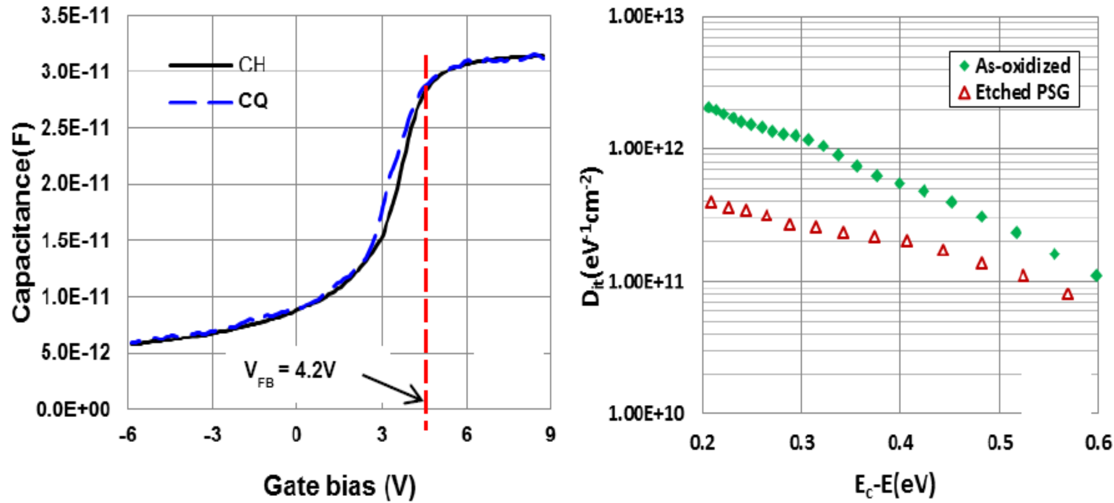

Fig. 3 Room temperature hi-low C-V curves **(a)** and interface trap density of the etched PSG MOS capacitor **(b)**.For comparison as-oxidized D_{it} is also included.

From results it can be inferred that after etching there is a loss of both phosphorous and nitrogen from the interface, which is shown to increase D_{it} at 0.2eV. As a result, we observe increased interface trap densities and flatband voltage 4.2V for these devices, although they have NO-like D_{it} (the unetched PSG MOS-C which is referred as PSG in this paper has V_{FB} close to 0V).

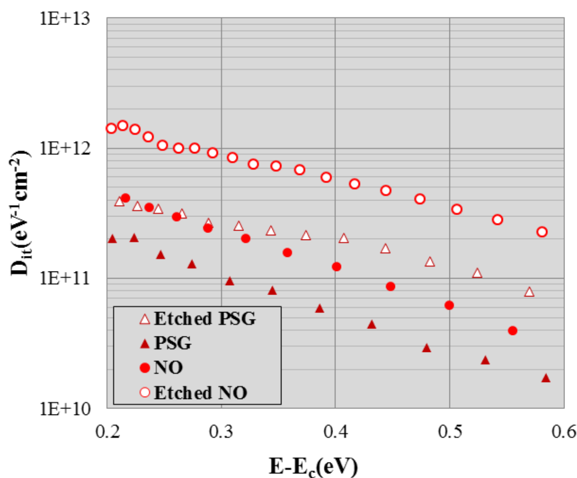

Fig.4 Interface trap density (D_{it}) before and after etching for NO and PSG MOS capacitors. D_{it} increases after etching, but etched PSG MOS-C is as good as NO passivated MOS-C.

(ii) BIAS-TEMPERATURE STRESS (BTS)

The results after BTS measurements for etched PSG MOS capacitors are shown in Fig 5. As we can see the shift in flatband voltage (ΔVFB = VFB, final-VFB,intial) is very large for non-etched MOS capacitors. There is a continuous decrease in ΔVFB from -1.2V to -16.5V with no sign of saturation even after ~2hr. This large negative shift is due to the presence of net positive charge at the interface caused by polarized PSG layer. The results for etched PSG MOS-C are shown by unfilled triangles (Fig 5). The PSG layer has been removed in BOE. There are two distinct feature of this device; ΔVFB is positive and smaller, and ΔVFB achieved saturation in less than 1hr. No negative shift in flatband voltage indicates the absence of net negative charge at the interface for etched PSG

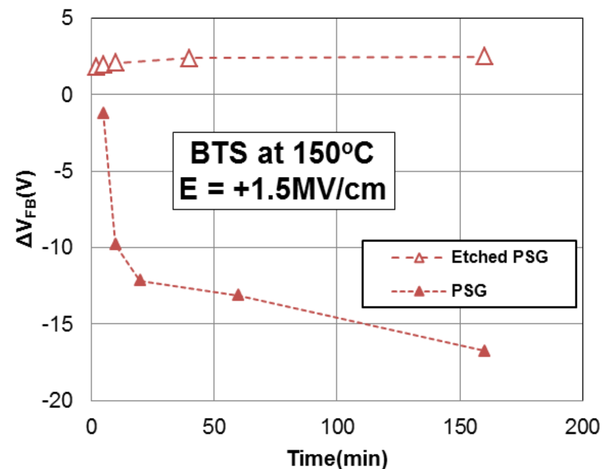

Fig.5 Shift in flatband voltage, $\Delta V_{FB} = V_{FB,final} - V_{FB,intial}$, of a PSG MOS-C before and after positive BTS. Device stability improves after etching.

MOS-C. The positive shift in V_{FB} for these devices is caused by electron-injection from oxide into SiC. This effect is well known in NO passivated MOS-C after positive BTS measurements (Lelis, Habersat, Green, & Goldsman, 2009). In PSG devices, polarization charge induces a negative shift in V_{FB} and this shift keeps increasing with stress time. But in the case of etched MOS-C, BTS results have shown that the etching of PSG layer improves the stability of MOS-C while keeping the passivation effect of phosphorous (D_{it} is still NO-

like). We offer a theory in the following section to explain this behavior.

(iii) X-RAY PHOTOELECTRON SPECTROSCOPY (XPS) OF THE 4H-SIC/SIO$_2$ INTERFACE

XPS results show that PSG layers can be completely removed by etching in BOE when the original SiO_2 layer is grown on Si substrate. In contrast, as shown in Fig 6(a), BOE does not completely remove the PSG layer from SiC. After hard etching (2-3 min is BOE), a 2-3nm Si-C-O-P interfacial layer can still be observed. The phosphorous areal density in this layer is around 2×10^{14} atoms/cm^2 (about one tenth of a monolayer). The areal density of phosphorus before etching is 10^{15}cm^{-2}. We lose P after etching which is consistent with higher trap density compared to PSG MOS-C (Fig 4) for the etched PSG sample as shown in Fig 6(a). Also, there is a right shift of 1eV in the binding energy of the P after etching. This suggests that P is in a different chemical environment at the interface compared to the bulk of the PSG layer. Fig 6(b) shows the XPS signals from 1s oxygen (O). The XPS analysis led to following conclusion. (i) Unetched phosphorous responsible for the “NO-like” interface trap density. (ii) Most of the positive polarization charge in the original PSG layer has been positioned near the interface but just outside the unetched layer and hence explains the increase in stability (smaller shift in ΔV_{FB}).

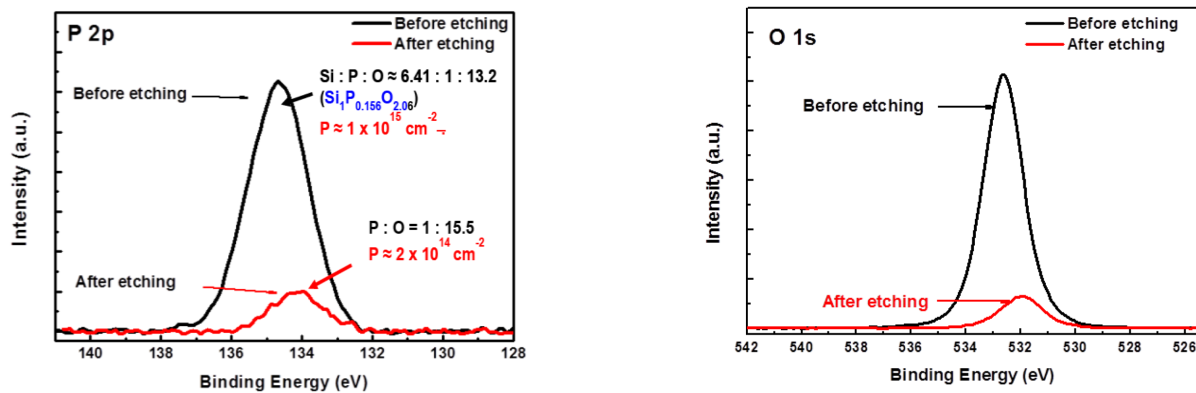

Fig. 6 (a) XPS phosphorous signal from a PSG layer on 4H-SiC before and after etching in BOE. The red signal corresponds to ~2×10^{14} P atoms/cm^2 (equivalent to ~ 0.1monolayer) in a Si-O-C-P interfacial layer that does not etch. No interfacial layer containing P is observed after etching PSG layers on Si (data is not shown) **(b)** XPS signal of 1s O from PSG before and after BOE etching.

CONCLUSION

In this paper we have proposed a new process to improve the stability of MOS-C devices after P passivation. With the etched PSG process not is the flatband voltage improved, but also the NO-like interface trap density is retained. The P left after etching is responsible for this improvement. All the fabrication steps are described in detail for the execution of the process.

ACKNOWLEDGMENT

This work was supported by the National Science Foundation, the U.S. ARL, and the II-VI Foundation.

REFERENCE

Chung, G., Tin, C., Williams, J., McDonald, K., Chanana, R., Weller, R. A., Das, M. (2001). Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide. *Electron Device Letters, IEEE, 22*(4), 176-178.

Cooper Jr, J. (1997). Advances in SiC MOS technology. *physica status solidi (a), 162*(1), 305-320.

CREE.(2014).C2M1000170D http://www.cree.com/Power/Products/MOSFETs/TO247/C2M1000170D.

Gupta, S. K., Singh, J., & Akhtar, J. (2012). *Physics and Technology of Silicon Carbide Devices*

Kern, W. (1990). The evolution of silicon wafer cleaning technology. *Journal of the Electrochemical Society, 137*(6), 1887-1892.

Kern, W. (1991). *Thin film processes II* (Vol. 2): Academic press.

Kern, W. (1993). Handbook of semiconductor wafer cleaning technology. *New Jersey: Noyes Publication*, 111-196.

Kurimoto, H., Shibata, K., Kimura, C., Aoki, H., & Sugino, T. (2006). Thermal oxidation temperature dependence of 4H-SiC MOS interface. *Applied Surface Science, 253*(5), 2416-2420.

Lelis, A. J., Habersat, D. B., Green, R., & Goldsman, N. (2009). *Temperature-Dependence of SiC MOSFET Threshold-Voltage Instability.* Paper presented at the Materials Science Forum.

Liu, G., Ahyi, A. C., Xu, Y., Isaacs-Smith, T., Sharma, Y. K., Williams, J. R., Dhar, S. (2013). Enhanced Inversion Mobility on 4H-SiC Using Phosphorus and Nitrogen Interface Passivation. *Electron Device Letters, IEEE, 34*(2), 181-183.

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Okamoto, D., Yano, H., Hatayama, T., & Fuyuki, T. (2010). Removal of near-interface traps at SiO 2/4H–SiC (0001) interfaces by phosphorus incorporation. *Applied Physics Letters, 96*(20), 203508-203508-203503.

Sharma, Y., Ahyi, A., Isaacs-Smith, T., Modic, A., Park, M., Xu, Y., .Williams, J. (2013). High-mobility stable 4H-SiC MOSFETs using a thin PSG interfacial passivation layer. *IEEE Electron Device Lett, 34*(2), 175-177.

Sharma, Y., Ahyi, A., Issacs-Smith, T., Shen, X., Pantelides, S., Zhu, X., Williams, J. (2012). Phosphorous passivation of the SiO< sub> 2</sub>/4H–SiC interface. *Solid-State Electronics, 68*, 103-107.

Vossen, J. L., & Kern, W. (1991). Thin film process II. *Academic Press, New York*, 181-186.

Xu, Y., Zhu, X., Lee, H., Xu, C., Shubeita, S., Ahyi, A., . . . Ceesay, S. (2014). Atomic state and characterization of nitrogen at the SiC/SiO2 interface. *Journal of Applied Physics, 115*(3), 033502.

Zhang, X. (2013). *Reliability and Irradiation Effects of 4H-SiC MOS Devices.* Vanderbilt University.

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